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## Executive Summary

*Advanced designs in OMAP3 application processors address the need for low power without sacrificing performance. Active power management adjusts a component's operating frequency or voltage requirements to only those levels necessary. Static power management involves keeping an idle system in a power-efficient state until further processing is required. Plus, Texas Instruments (TI) has developed a number of external voltage regulators that lower the cost of implementing these power-saving features and reduce design time.*

*In this white paper, we'll review the concepts behind these various power-saving techniques, quantify the kinds of power savings that you can achieve with each, and discuss external power-management devices and power ICs that help multimedia processors reap the full benefits of these techniques.*

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# Power-Management Techniques for OMAP35x Applications Processors

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## New Methods of Power Management

Power consumption and battery life remain central factors in the development of portable electronic appliances; a multimedia processor is often the most power-hungry device in such systems. Two common ways to reduce CPU power requirements is to lower the clock rate at which an entire device operates or to lower the voltage, but this can affect system performance. Meanwhile, creative chip designers have come up with a variety of innovative on-chip methods to reduce power without adversely impacting system performance.

TI's OMAP35x processor optimizes system power consumption by employing two main techniques: managing active system power consumption and managing standby system power consumption.

- **Active power consumption management** – Used to optimize the power a system draws while processing data to achieve useful results. Here, three basic methods exist:
  - Dynamic voltage and frequency scaling (DVFS)
  - Adaptive voltage scaling (AVS)
  - Dynamic power switching (DPS)
- **Static power consumption management** – Keeps an idle system in a power-efficient state until further processing is required. Managed by a technique known as static leakage management (SLM), static power consumption can result in several low-power modes, from standby to a deep sleep mode, which mimics the power-off state but has faster wake-up latency.

## DVFS

With DVFS, clock rates and voltages are lowered by software based on the performance requirements of the application. For each operating performance point (OPP), software sends control signals to external regulators in order to set the minimum voltage.

With an OMAP35x device, DVFS is applicable to two voltage supplies: VDD1 or VDD\_MPU\_IVA, which supplies the DSP and ARM processors (see Figure 1, next page) and VDD2 or VDD\_CORE, which supplies the interconnects between subsystems and peripherals (see Figure 1, next page). These two rails consume most of the chip's power, typically around 75 to 80 percent.

OMAP 35xx	OPP	ARM MHZ	DSP MHZ	VDD1	OPP	L3 MHz	VDD2
	5	650	430	1.35	3	166	1.15
	4	550	400	1.27	2	100	1
	3	500	360	1.2	1	41.5	0.95
	2	250	180	1			
	1	125	90	0.95			

*Figure 1. Predefined operating performance points (OPPs) for the OMAP35x for VDD1 controlling the ARM's speed (left) and VDD2 for the L3 system-interconnect clock (right).*

For instance, even though the ARM component in an OMAP35x processor can run at rates as high as 600 MHz (for OMAP3503, OMAP3515, OMAP3525 and OMAP3530), not all of that computational power is required in every case. Thus, the software selects the predefined OPP that is guaranteed to result in the ARM running at a certain minimum rate, thus meeting system frequency requirements. Note that future devices stemming from the OMAP3 platform may have higher frequencies.

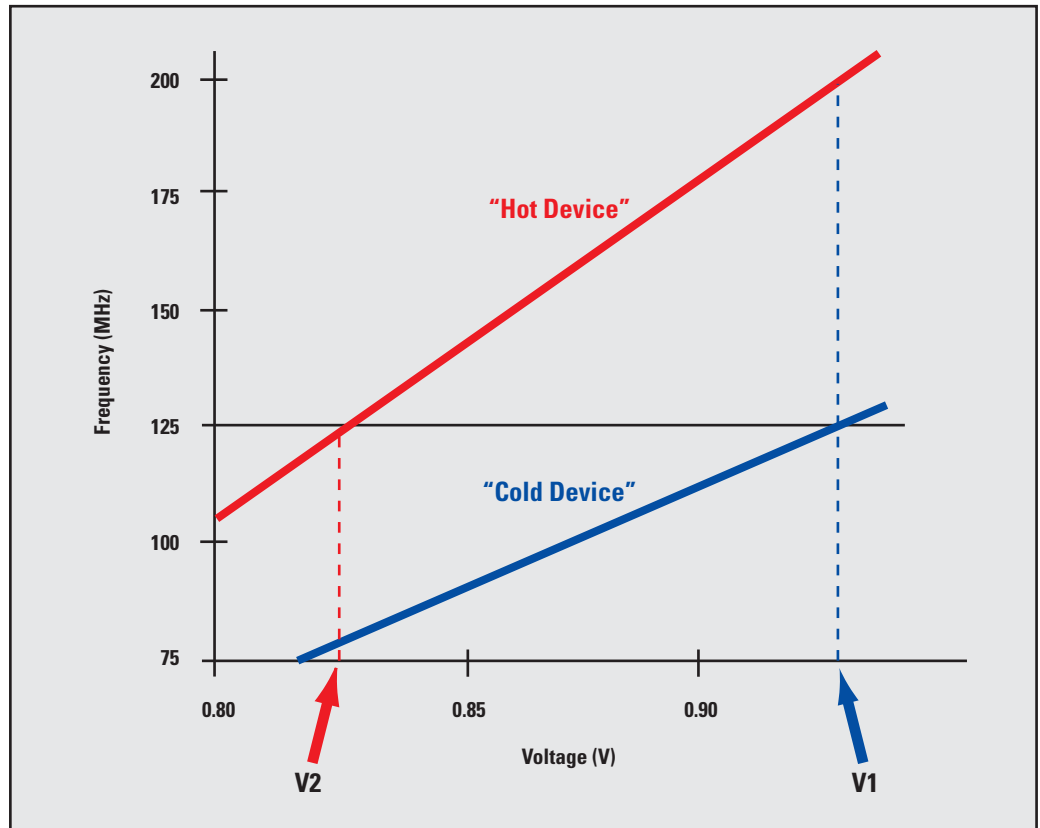
In this way, DVFS makes a large contribution toward optimizing power usage. For instance, you can decode MP3s with plenty of margin for other tasks by transitioning the processor into a low OPP, where the ARM can run as high as 125 MHz. To achieve that functionality with optimal power consumption, it is possible to lower VDD1 to 0.95 V for that rate, as opposed to the maximum of 1.35 V, which supports up to 600-MHz operation.

## AVS

The second active power management technique in OMAP35x processors is AVS, which is implemented with a technique known as SmartReflex™ technology. It is based on variations that inevitably come up during chip manufacturing as well as during a device's operational lifetime.

The silicon manufacturing process yields parts with a distribution of performance capabilities; for a given frequency requirement, some devices (known as “hot,” “strong” or “fast” devices) can achieve that frequency with a lower voltage than can “cold” (also called “weak” or “slow”) devices. Here, AVS comes into play—the chip senses its own performance level and adjusts voltage supplies accordingly.

Dedicated, on-chip SmartReflex technology-based hardware implements a feedback loop that does not require processor intervention, which dynamically optimizes voltage levels to account for variations in process results, temperature and silicon degradation (Figure 2, next page). Software sets up the SmartReflex technology-based hardware for each OPP. The hardware control algorithm then sends commands to external voltage regulators over an I<sup>2</sup>C bus, lowering the appropriate regulators' outputs in incremental steps until the processor just exceeds target frequency requirements. SmartReflex technology-based AVS works in concert with DVFS to provide additional power savings beyond those obtainable by DVFS alone.



*Figure 2. Processors come off the fab line with different performance characteristics. Here, a “cold” OMAP35x device needs 0.94 V to run at 125 MHz, whereas a “hot” device needs just 0.83 V to run at the same frequency. Adaptive voltage scaling (AVS) includes a SmartReflex technology-based feedback loop that can lower supply voltages from the safe 0.95-V level (set initially under the DVFS policy) to the frequency levels individual devices need to run specific processing tasks.*

For example, you might start by designing in a voltage that fits all cases; for 125 MHz, that is 0.95 V (V1 in Figure 2). If a hot OMAP35x device with SmartReflex technology is inserted in the system, however, the on-chip feedback mechanism can automatically lower the voltage of the ARM to 0.85 V or less, yet have the same 125-MHz performance (V2 in Figure 2).

**DPS** Although these first two methods of active power management find the minimum operating voltage necessary to run part of an OMAP35x device at the desired speed, DPS essentially determines when part of a device has completed its current computational tasks, is not needed at the moment, and puts it into a low-power state (Figure 3, next page).

For example, an OMAP35x can enter a low-power state while waiting for a DMA transfer to finish. When it is time to process the data again, the processor wakes up to its normal state, with wake-up latencies on the order of microseconds.

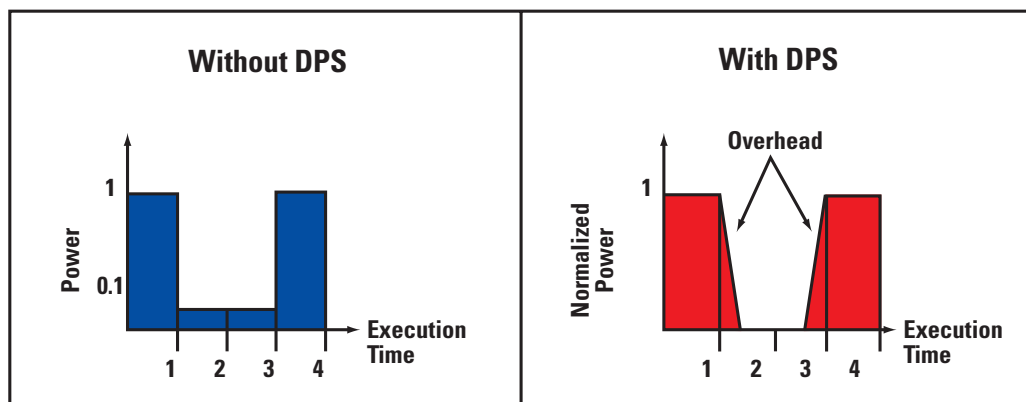


Figure 3. In dynamic power switching (DPS), parts of an OMAP35x device switch to a low-power state after completing their tasks.

### Static/Passive Power Management

Although the DPS puts only a section of an OMAP35x multimedia system-on-chip (SoC) in a low-power state, there are situations where it makes sense to put the entire device in low-power mode – either automatically when no application is running or upon user request.

The mechanism for doing this is called SLM, which initiates standby or device-off mode. One key difference between the two modes is that in standby mode, the OMAP35x retains internal memory and logic, whereas in device-off mode the system state is saved in external memory.

With SLM, the wake-up time is far faster than a cold boot because the program is already loaded in external memory; you do not have to wait for a full operating system (OS) restart. An example of using SLM would be in a media player that, following 10 seconds of on time with no processing and no user input, shuts off the display and enters standby or device-off mode.

When looking at OMAP35x devices, the device-off mode is the lowest power mode in which the device can wake up autonomously. Here, all power domains are off except for the wake-up domain; power consumption arises only from wake-up domain operation and I/O leakage. The system clock is turned off; therefore the wake-up domain is separately clocked at a slow 32 kHz. Also, no memory or logic is retained inside the processor, as all power is internally turned off.

The OMAP35x can also automatically send signals to external regulators that can be turned off during this deep sleep state. The system state is saved in external memory before entry into the device-off mode; after a post wake-up reset, the microprocessor unit (MPU) jumps to a user-defined function and the SDRAM controller configuration is restored from minimal memory kept inside the wake-up domain.

## Application Techniques

By combining these power management techniques, it is possible to handle a variety of operating scenarios in an optimal manner. As shown in Figure 4 when system activity on a portable multimedia player is high – such as when viewing high-resolution video – an overdrive OPP can be set on VDD1.

For Web browsing that requires medium power consumption, nominal OPPs can be set for VDD1 and VDD2. For listening to music, which has relatively low-power demands, the lowest OPPs can be set for VDD1 and VDD2. In all three of these examples, you can activate SmartReflex technology to flatten power consumption differences between “hot” and “cold” devices.

When the user leaves the media player on but does not use it for several hours or days, SLM can automatically drop into device-off mode.

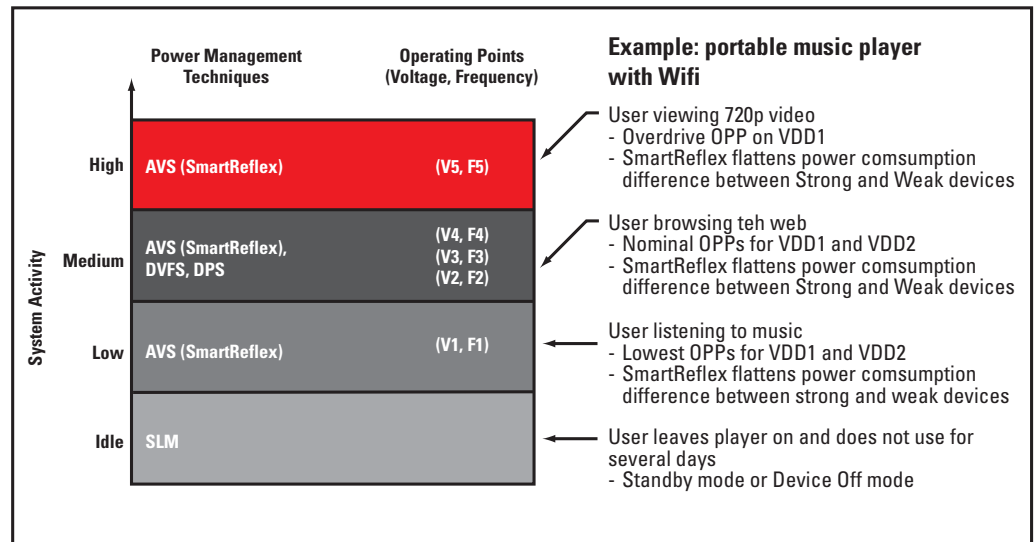


Figure 4. By combining various power-management techniques, it is possible to handle a wide range of system activities based on user requirements.

To get a more specific idea of the power savings possible by taking advantage of these features, consider several typical use cases using an OMAP35x. The following examples do not utilize AVS/SmartReflex technology unless otherwise noted. In these descriptions, IVA refers to the image, video and audio accelerators subsystem, including the DSP.

### Device-Off Mode: 0.590 mW

This is the lowest power mode from which the OMAP35x device can still wake up autonomously. In this mode, the entire device except for the wake-up domain is off, and the wake-up domain runs lower than 32 kHz. Unused regulators are turned off (VDD1 = VDD2 = 0), SDRAM is self-refreshed, and a special boot sequence restores the SDRAM controller and system state upon wake up.

### Standby Mode: 7 mW

In this device state, the wake-up domain is active while all other non-wake-up power domains are in low-power retention (VDD1 = VDD2 = 0.9 V). All logic and memory are maintained. AVS is off.

**Audio Decode: 22 mW  
(Excluding DPLL  
and I/O Power)**

The ARM, although running at 125 MHz, merely sets up DMA to read input data from a multimedia card, after which it goes into a sleep state. The IVA decodes MP3 frames (44.1 kHz, 128k bps stereo) and sends decoded data to buffers located in SDRAM. An on-chip multichannel buffered serial port sends data to an audio codec for playback. As for system configuration, the DSP runs at 90 MHz and transitions into low power states to save power when cycles are not required for processing ( $VDD1 = 0.9\text{ V}$  and  $VDD2 = 1\text{ V}$ ).

**Audio/Video Encode:  
540 mW (Excluding  
DPLL and I/O Power)**

In this case, audio is captured and encoded (AACe+ at 48 kHz and 32k bps stereo), video is captured and encoded (H.264 VGA resolution at 20 frames/sec, 2.4 Mbps), both are stored, and at the same time video is displayed. In this configuration, the ARM runs at 500 MHz, the DSP runs at 360 MHz and  $VDD1 = 1.2\text{ V}$  and  $VDD2 = 1.15\text{ V}$ .

An on-chip camera subsystem captures video input coming from an external sensor, a multichannel buffered serial port captures audio PCM input, the IVA performs video and audio encoding, the encoded data is stored in a multimedia card, and the display subsystem rotates the video and sends it out on LCD and TV output interfaces.

Let's examine how the OMAP35x implements these power-management functions. First note that the device is partitioned into three major domain schemes:

- **Clock domains** – modules are fed with the same clock, gated independently.
- **Power domains** – modules are fed with the same power rail, controlled by independent power switches.
- **Voltage domains** – modules are supplied by the same voltage regulator, whether embedded or external.

This partitioning of the device into domains with separate control points enables the DPS and SLM power management features. This architecture also permits key techniques like DVFS and AVS at the two voltage domains where these features can provide the maximum benefits. The crucial OMAP35x component that controls this infrastructure is the power reset and clock manager (PRCM).

Two kinds of clocks are provided to the modules. First are interface clocks, which ensure communication between a module and the system interconnects; they are used to read and write module registers. Second are functional clocks, which supply the functional part of a module or subsystem. Note that a module or subsystem may require several functional clocks, all of which can be gated automatically by the PRCM when not being used.

Power domains can be placed into one of four states, as shown in Figure 5. The state depends on the domain clock activity and the state of the power supplied to the logic and memory (separately switchable in some power domains).

Power State	Power		Clocks
	LOGIC	MEMORY	
<b>ACTIVE</b>	<b>ON</b>	<b>On, RETENTION or OFF</b>	<b>ON (at least one)</b>
<b>INACTIVE</b>	<b>ON</b>	<b>On, RETENTION or OFF</b>	<b>OFF</b>
<b>RETENTION (CSWR)</b>	<b>ON</b>	<b>RETENTION or OFF</b>	<b>OFF</b>
<b>RETENTION (OSWR)</b>	<b>OFF/RFF</b>		
<b>OFF</b>	<b>OFF</b>	<b>OFF</b>	<b>OFF</b>

*Figure 5. In OMAP35x devices, there are four possible power states that depend on power supplied to logic and memory as well as the clocks. These states are active, inactive, retention and off, respectively, in decreasing order of power consumption. For additional power savings, some domains have the option of saving some off logic state in retention flip-flops (RFFs) and then cutting off power to the domain logic. Turning off power to the logic is the difference between open switch retention (OSWR) and closed switch retention (CSWR).*

To achieve this extensive power-management flexibility, the DSP processor relies on the on-chip power reset and clock manager (PRCM) mentioned earlier. More specifically, the OMAP3530 processor divides its functional blocks into 18 power domains, each with its own switch. The PRCM can switch all the power domains, but many of them can also be user-controlled.

As a further power-management measure, TI provides several classes of SmartReflex technology-based operation on its devices, and Class-3 is available on OMAP35x devices. As described earlier, the SmartReflex technology-based subchip has a dedicated hardware loop to dynamically optimize the voltage for process, temperature and silicon degradation effects; MPU intervention is not required.

Software sets up a SmartReflex technology-based subchip for each OPP; a hardware voltage processor is used in auto mode at an OPP. Adjustments around an OPP are sent to the voltage regulator automatically using the I<sup>2</sup>C4 bus.

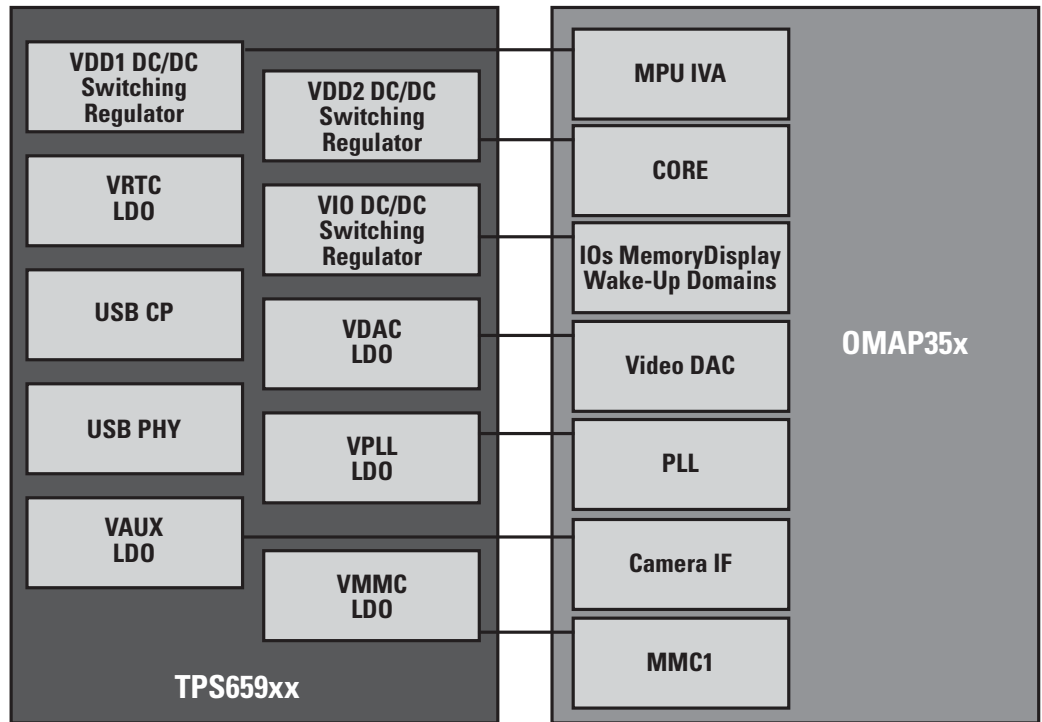
### **Specialized Voltage Regulators**

These states require coordination with the auxiliary voltage regulators typically needed for OMAP35x devices. Many regulators on the market can do the job, but each must meet the processor's voltage, current and power slew rate specifications, as well as power up/down sequencing requirements.

In order to implement DVFS and AVS operations on OMAP™ processors, the associated regulators must also have I<sup>2</sup>C programmability. Finally, for device-off mode, it must be possible to turn the VDD1 and VDD2 regulators on and off, either with I<sup>2</sup>C commands issued automatically or by a dedicated GPIO signal. The latter option brings a slightly faster wake-up time because there are no I<sup>2</sup>C latencies.

TI has developed a number of single- and multiple-output voltage regulators – with features designed specifically to meet the needs of OMAP35x processors – that are capable of DVFS and SmartReflex technology through their I<sup>2</sup>C buses. These processors have several voltage domains supplied by external resources and that condition power taken from a common battery.

The difference between the OMAP35x power solutions resides in the amount of integration within each device. The TPS62350 (a tiny, 3-MHz, single-output DC/DC converter) and TPS65023 (multi-output DC/DC converter) offer the greatest flexibility in system optimization. Going a step further are parts in the TPS659xx family, which along with multi-output DC/DC converters including audio, a USB OTG PHY and dual I<sup>2</sup>C ports communicate with the OMAP35x device.



*Figure 6. Advanced voltage-regulator chips incorporate the functions of multiple individual switching regulators and low-dropout linear regulators (LDOs), in this case handling all of the different voltage domains for the OMAP35x processor. This level of integration considerably eases system development while allowing designers to take advantage of maximum power efficiency.*

## Conclusion

System designers and users are no longer restricted to just one or two power solutions. Today, with the high power management flexibility in advanced multimedia processors and support chips, designers can now dynamically select from a range of choices for optimal power consumption to fit any use case.

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