

RF-sampling tool kit for system designers

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Introduction

System designers are moving toward direct radio-frequency (RF) sampling for two reasons. The first is that they may be designing a receiver that is digitizing more instantaneous bandwidth (IBW). Such cases don't require much additional design consideration, as the system still looks like an intermediate-frequency (IF) sampling architecture, except with a wider bandwidth. As the IBW increases, so does the sampling rate of the analog-to-digital converter (ADC). Eventually, it reaches the gigasamples-per-second range and the system looks like RF sampling.

The second reason that designers may also choose a direct RF-sampling architecture in an effort to reduce system size and power by removing an entire down-conversion stage. In this case, the IBW is much smaller than the ADC's Nyquist zone and frequency planning can help optimize system performance.

This article describes three basic tools that can help system designers in both the design and debugging of direct RF-sampling receivers:

- Frequency planning calculator
- Analog Filter tool
- Digital decimation-filter (DDC) spur locator

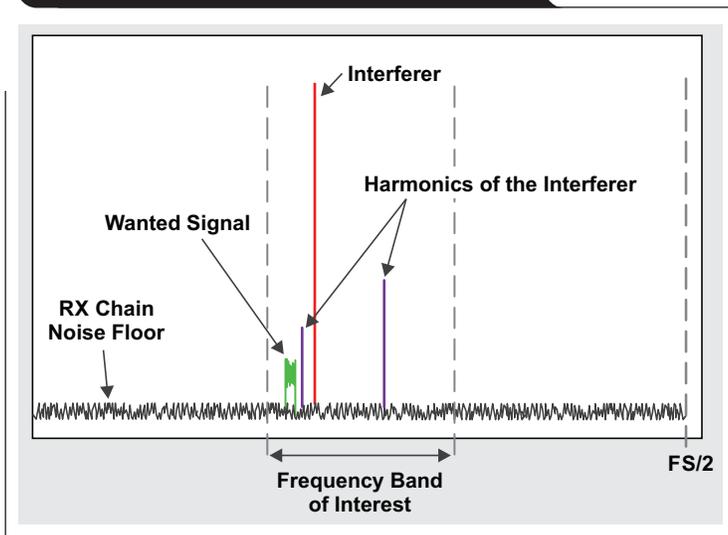
See Reference 1 at the end of this article for the free download link to these tools.

In the concept phase, a frequency planning tool enables fine-tuning of both the ADC sampling rate and input-frequency location in order to optimize the spurious-free dynamic range (SFDR) during a blocking event. Some designs have flexibility on both; others, such as a L-band receiver or a wireless-infrastructure base station, may deal with fixed-frequency bands and only offer sampling-rate tuning.

The response of the external RF filter is highly dependent on both the system SFDR targets and the SFDR performance of the ADC itself; an analog filter tool can help predict response problems during the design phase.

The decimation-filter spur-locator or DDC tool helps in situations where unwanted spurs in the fast-Fourier transform (FFT) spectrum occur when bringing up the system. When the ADC outputs the entire Nyquist zone, it's simple to determine the original frequency, but not necessarily the source of the spur. However, once digital decimation with complex mixing comes into play and only a partial FFT spectrum (into which the spurs are folded) is available, this simple tool maps original spurs of the ADC to their new locations.

Figure 1. A weak wanted signal in the presence of a strong in-band interferer



Frequency planning calculator

When I'm doing frequency-planning analysis for a specific customer scenario with one of TI's RF-sampling data converters, the Frequency Planning worksheet of the tool is used to analyze possible effect of unwanted harmonics.

The basic idea is to adjust the ADC sampling rate and/or the input frequency range so that harmonics generated from an in-band blocker (which can't be filtered out) fall outside the frequency band of interest. For example, consider a radar receiver where an in-band jammer makes it through the front-end RF filters and then shows up in the spectrum of interest as shown in Figure 1. The large power of the interferer limits how much gain can be applied in the receiver chain (avoiding saturation of the ADC input) to detect weak target reflections. Furthermore, the interferer also generates harmonics in the analog RF signal chain and ADC (the second harmonic (HD2), for example), which can limit the receiver's ability to detect weak signals if the weak signals fall in band.

The frequency planning calculator is very simple to use. It requires user entry for the ADC sampling rate and ADC interleaving factor, as well as the bandwidth and center frequency of the signal of interest. The tool then calculates any potential overlap of harmonics with the wanted signal and provides a graphical representation of the entire Nyquist zone of the ADC of where the harmonics fall after aliasing.

The example in Figure 2 shows an optimum frequency plan for a 100-MHz band centered at 2.05 GHz with a clock rate (FS) of 2.9 Gsps, where none of harmonics overlap with the wanted signal. The HD2 and HD3 images are mixing products of the second and third harmonic with the core ADC clock rates (FS/2 for a 2x interleaved ADC). These spurs are about 10 to 15 dB better than HD2 and HD3.

On the other hand, a center frequency of 1,950 MHz results in the non-optimum frequency plan shown in Figure 3, where the band of interest overlaps with the HD2 of the interferer. The overlap field is shaded red for overlap of HD2 or HD3, which are typically the worst spurs of an ADC.

Figure 2. Example of an optimum frequency plan

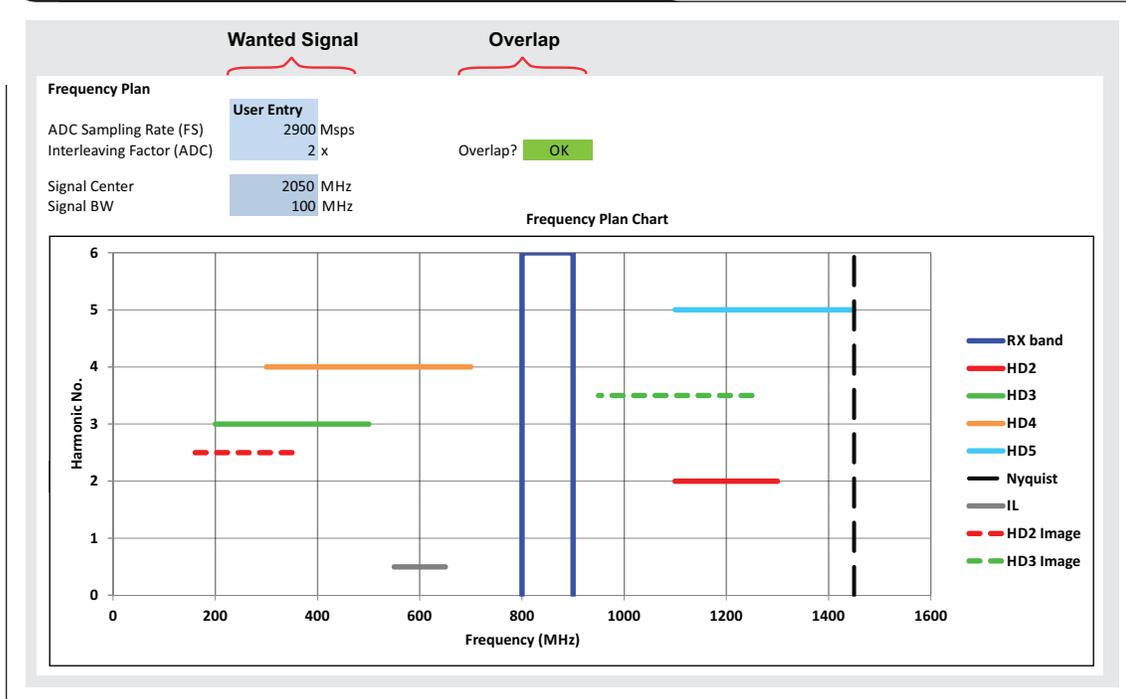
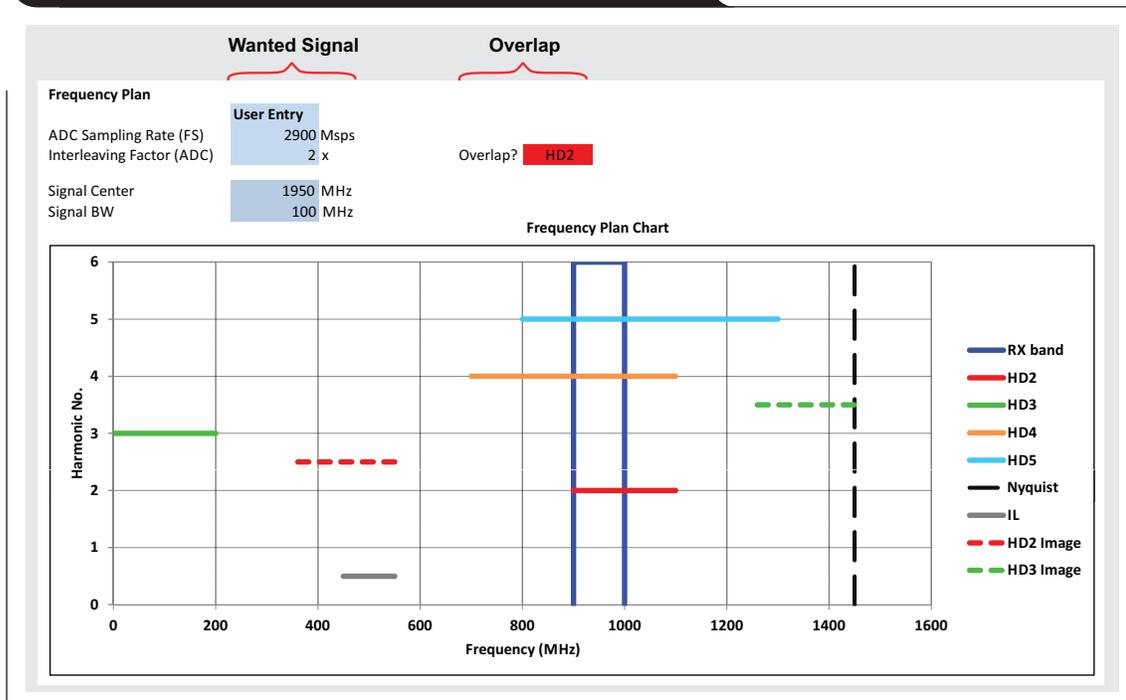


Figure 3. Example of a non-optimum frequency plan



As applications such as wireless base stations move into multiband scenarios, the frequency planning tool also includes a F-Band MB worksheet for multiband as well.

Analog filter tool

The external out-of-band RF filter requirement is based on the in-band SFDR requirement. Because there is no possibility of frequency planning around the out-of-band blocker, the amplitude of the blocker must be attenuated through the filter such that the resulting in-band spur is below the desired in-band SFDR requirement. For example, if the SFDR limit is 100 dB and the HD2 performance of the ADC is 65 dB, then the frequency location where the HD2 of the out-of-band blocker falls in-band needs 35 dB of attenuation.

The analog filter tool sweeps the blocker location from 1 MHz to 4 GHz and generates a filter mask based on the desired SFDR limit and entered ADC SFDR specs. It then generates a graphical representation of attenuation versus frequency, while a table illustrates the “close-by” filter requirements (see Figure 4). Certain scenarios require a large close-by filter requirement that may not be realistic, so the table offers a good first-cut estimate. The tool also shows a large filter requirement for the alias, where a blocker in the adjacent Nyquist zone requires attenuation equal to the SFDR requirement.

The analog filter tool does not take into account that HD2 improves by 1 dB with 1-dB back-off. But if the blocker amplitude can be larger than the ADC at full scale, additional attenuation is required to prevent saturating the ADC.



Decimation filter spur locator (DDC tool)

The internal decimation filter of the RF-sampling ADC typically reduces excess bandwidth and thus the amount of digital data that needs transferring. However, when trying to optimize the performance of the analog system during initial system start-up, it can be difficult to track down the original spur frequency/location if only a partial FFT spectrum from the output of the decimation filter is available.

The DDC tool calculates spur locations before and after complex decimation in order to easily identify spurs in the output spectrum. The tool processes both the primary signal alias (between DC and FS/2) as well as the negative image (between -FS/2 and DC but shifted to FS/2 and FS). The inputs required are ADC sampling rate, interleaving factor, input frequency, complex decimation setting and numerically controlled oscillator (NCO) frequency.

The setup data and results shown in Figure 5 have the

ADC sampling rate, FS = 3 GSPS (4x interleaving); the input frequency, FIN = 2.1 GHz; and the complex decimation by 4 with NCO = 2.2 GHz. The DDC tool uses the setup configuration data to show the calculation results as a table and as a graphical representation of the output spectrum that the ADC would provide. The results table also shows the individual spur locations after sampling, after the NCO shift, and after decimation.

After sampling, the 2.1-GHz input signal aliases to 900 MHz. Since the NCO frequency inside the ADC is between 0 Hz and FS, the negative image -FIN (-900 MHz) shifts by +FS to 2,100 MHz (-900 MHz + 3 GHz = +2,100 MHz).

Figure 5 shows the decimation filter response centered around the 2.2-GHz NCO frequency. The data results after the NCO shift are shown in the shift-by-NCO column in Figure 5. Results are highlighted in red to indicate which spurs are inside the decimation filter passband and don't get attenuated.

Figure 5. DDC—Decimation filter spur-locator tool showing frequency spectrum after sampling

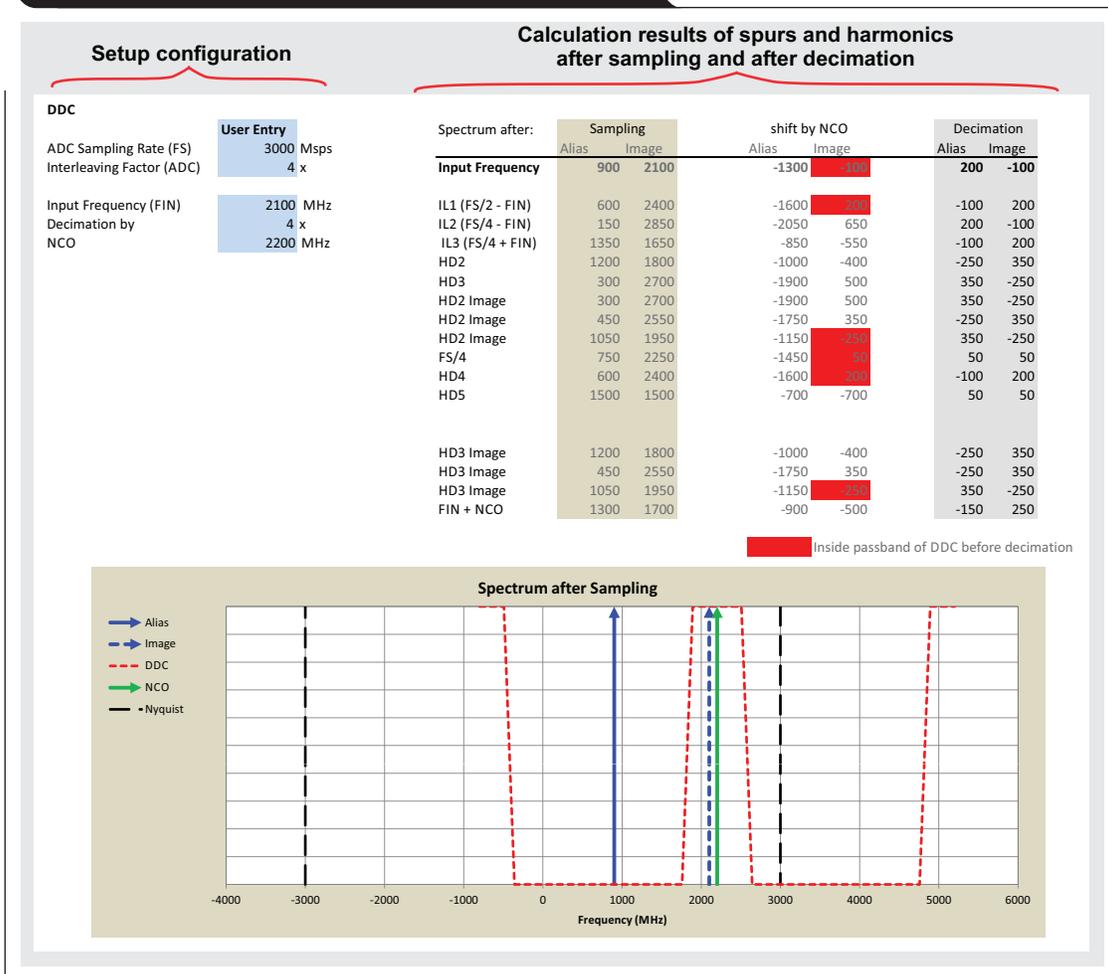
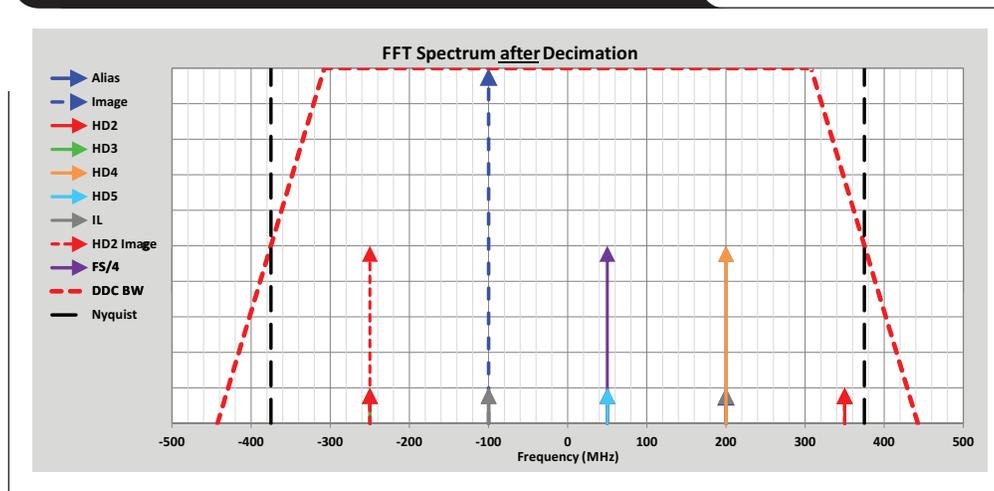


Figure 6. DDC—Frequency spectrum after decimation



In Figure 6, the graphical representation also shows attenuated spurs (lower amplitude) and spurs inside the filter passband (higher amplitude).

Conclusion

More than ever, system designers are now considering a modern system architecture that use a direct RF-sampling receiver. The three tools described in this article can greatly assist designers during the preliminary design stage to decrease development time.

Reference

1. “RF-Sampling Frequency Planner, Analog Filter, and DDC Excel™ Calculator,” design tool for data converters, Texas Instruments (FREQ-DDC-FILTER-CALC), 2017

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